MANUAL CONTROLS

The function of the individual manual oontrols is described in the Indications and Manual Controls section. However, when working through the ROS MAP chart many tests require observation of the output word at the sense latches from a forced ROAR address. This is best achieved by using a combination of the manual controls as follows:-

1. Rate switch to Single Cycle (to give a hardstop condition).
2. Set required address on manual data keys.
3. General Display and Store Switch to ROAR.
4. Push associated toggle switch to Store.

The result of this action will be to force the address set on the data keys into ROAR and, read out the associated word into the sense latches. The T clock will not be started.

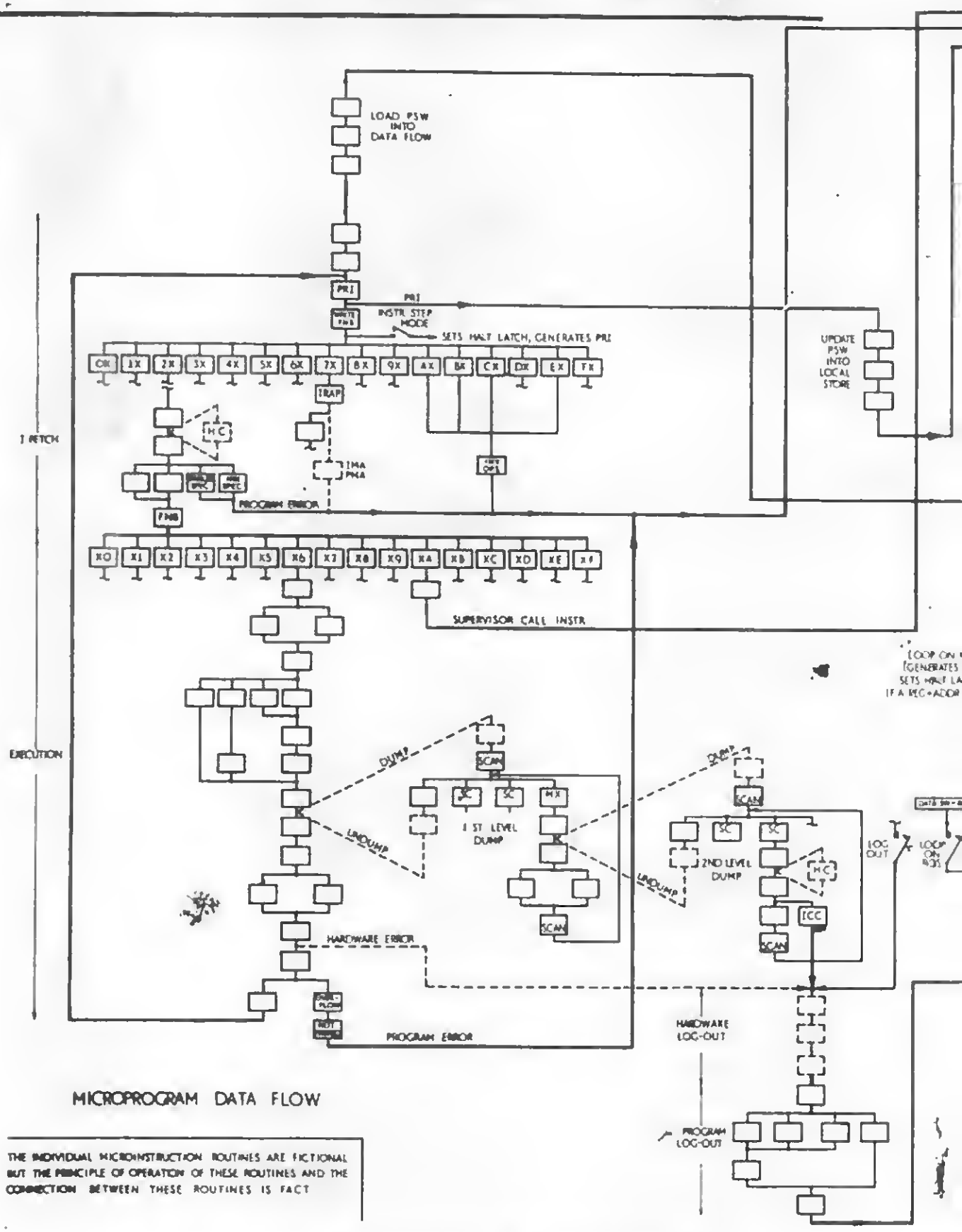
DIAGNOSTIC FACILITIES

Two special words are provided in ROS to facilitate fault finding. They are:-

1. At address 00800 is a word containing all 1's. Calling this word will give wrong address parity and wrong word parity.
2. At address 00400 is a word containing all o's. Calling this word will give correct address parity but wrong word parity. By manually selecting these words diagnostic evidence of the functioning of the ROS may be obtained.

MECHANICAL PACKAGING DESIGN

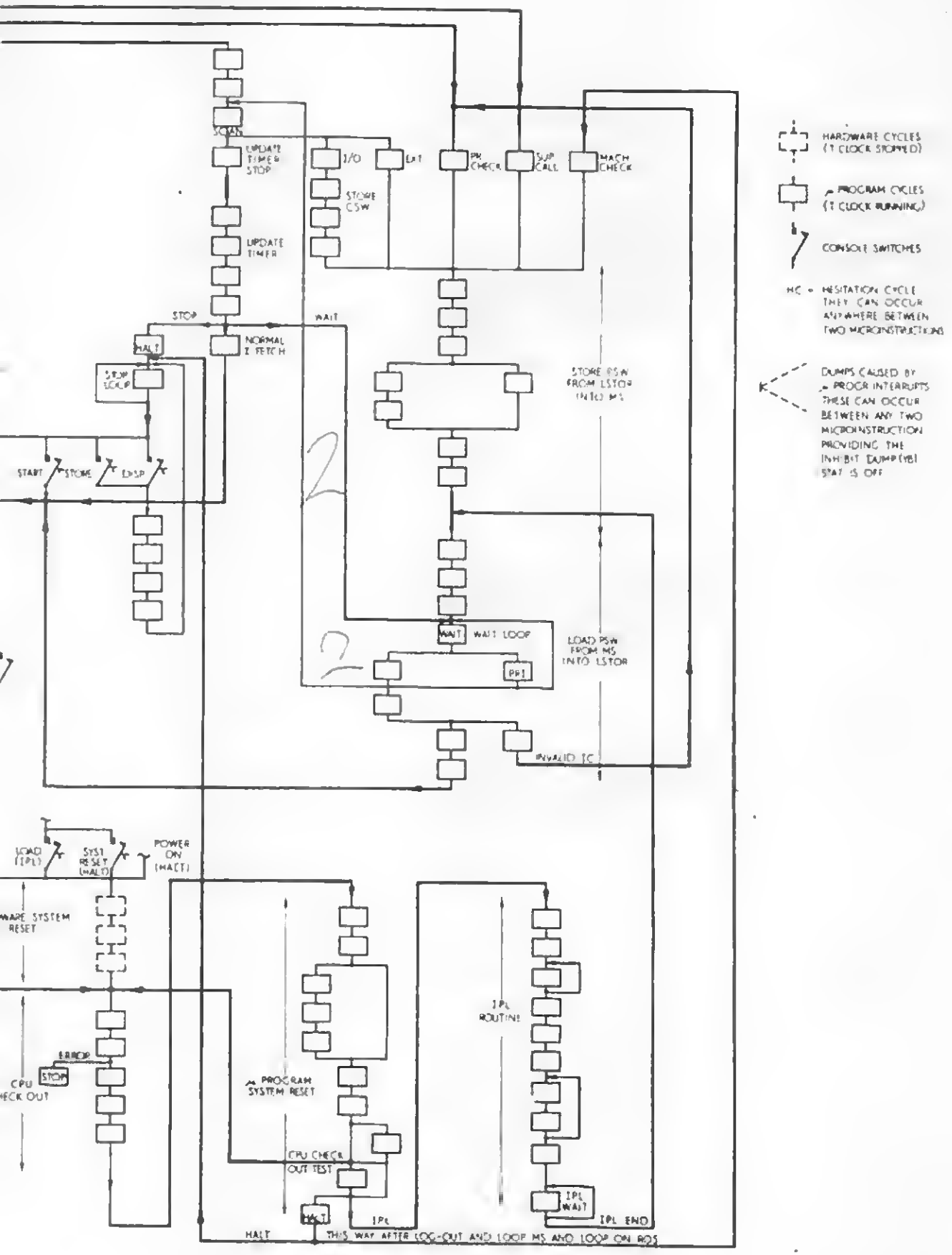
Refer to Volume 4 Section 6.



MICROPROGRAM DATA FLOW

THE INDIVIDUAL MICROINSTRUCTION ROUTINES ARE FICTIONAL BUT THE PRINCIPLE OF OPERATION OF THESE ROUTINES AND THE CONNECTION BETWEEN THESE ROUTINES IS FACT

IBM 360 MODEL 40 MICROPROGRAM DATA FLOW


SCAN
UPDATE TIMER & STOP
I/O
EXT
PI CHECK
SUP CALL
MACH CHECK
STORE CSW
UPDATE TIMER
STOP
WAIT
HALT
NORMAL I FETCH
STOP LOOP
START
STORE
DISP
STORE PSW FROM LSTOR INTO MS
WAIT
WAIT LOOP
PRI
LOAD PSW FROM MS INTO LSTOR
INVALID IC
LOAD (IPL)
SYST RESET (MALT)
POWER ON (MACT)
ERROR
STOP
PROGRAM SYSTEM RESET
CPU CHECK OUT TEST
MACT
IPL
IPL ROUTINE
IPL WAIT
IPL END
HALT
THIS WAY AFTER LOG-OUT AND LOOP MS AND LOOP ON ROS
HARDWARE CYCLES (T CLOCK STOPPED)
PROGRAM CYCLES (T CLOCK RUNNING)
CONSOLE SWITCHES
HC = HESITATION CYCLE THEY CAN OCCUR ANYWHERE BETWEEN TWO MICROINSTRUCTIONS
DUMPS CAUSED BY PROGR INTERRUPTS THESE CAN OCCUR BETWEEN ANY TWO MICROINSTRUCTION PROVIDING THE INHIBIT DUMP(YB) STAT IS OFF

a) CPU/HSSC Checkout

Execution of this microprogram will occur in the parent Processor. The Main Storage addressing tests, which use a test address less than 4096 will access a MS location determined as follows.

With the Share/Integral switch set to SHARE, the effective address will be the test value OR'ed with the prefix addressed by the Prefix Select Switch, i.e. MAIN or ALTERNATE, which will indicate access to the Main or Alternate Main Store. It is thus possible to access the remote Main Store under these conditions.

With the Share/Integral Switch set to INTEGRAL UPPER or INTEGRAL LOWER, the "Home" Prefix will be used. This is the prefix stored in the processor which detects the malfunction or which contains the System Reset, Load or Logout pushbutton which has been depressed. The state of the Prefix Select Switch will be ignored in this case. Thus, the Integral (Home) Main Storage will be accessed at the location obtained by ORing the test address with the Home Prefix.

b) Main Storage Diagnostic

Depending on the value of the prefix and of the state of the Prefix Select Key, teste may not be made for locations < 4096. This area of MS may be tested by changing the Prefix Card to one giving a prefix of zero. This change can be made by the CE in 5 minutes.

Addressing tests on locations < 4096 will operate with modulo 4096 data in adjusted MS locations of (Basic Address) OR (Prefix).

If the Share/Integral switch is set to SHARE, both Main Storages will be accessed from the one ROS.

Diagnosis of the integral MS only will be achieved with the Share/Integral switch set to the INTEGRAL LOWER state.

c) Local Storage Diagnostic

The Feature has no impact on this diagnostic.

Unknown, not sure if part of 360/40

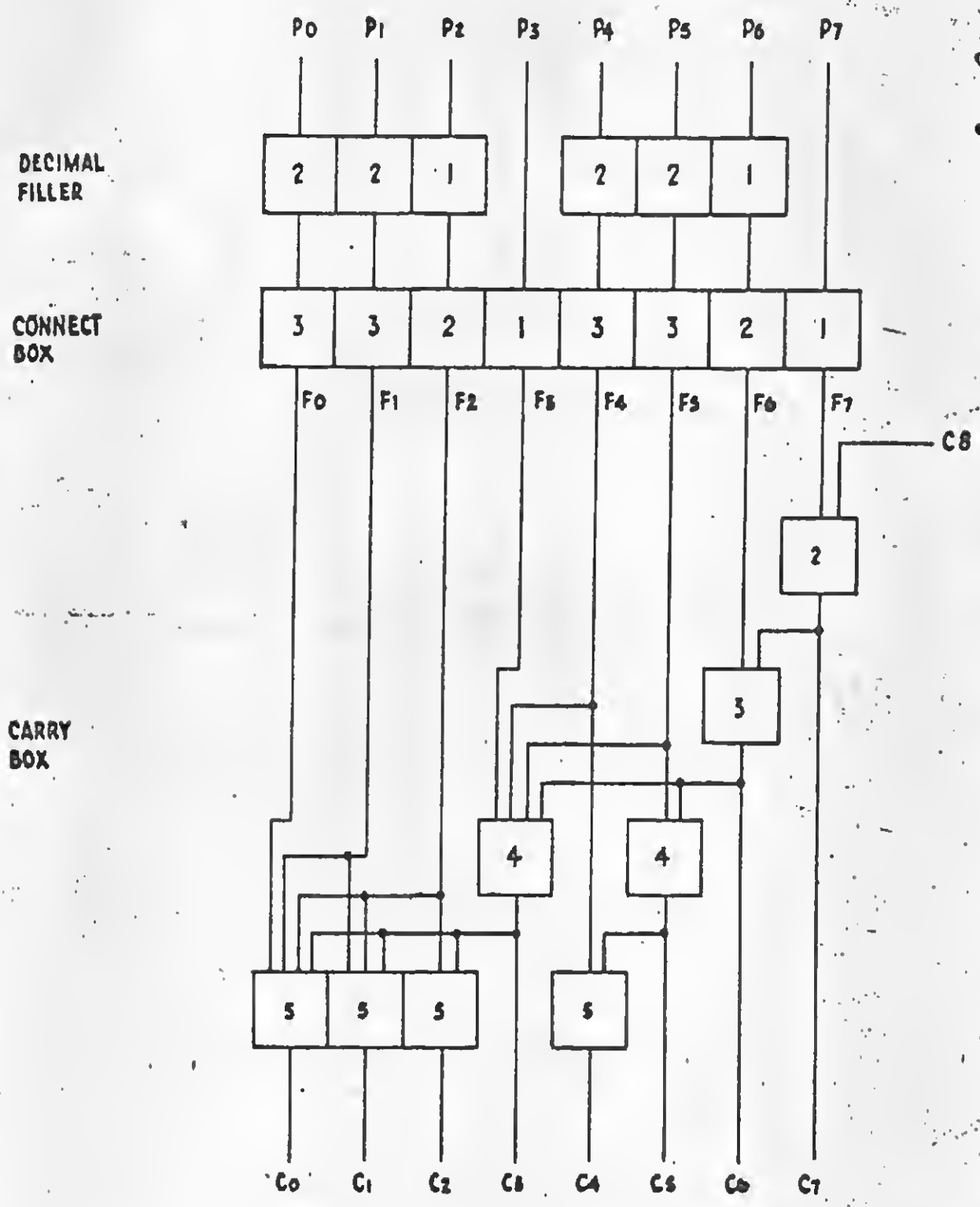


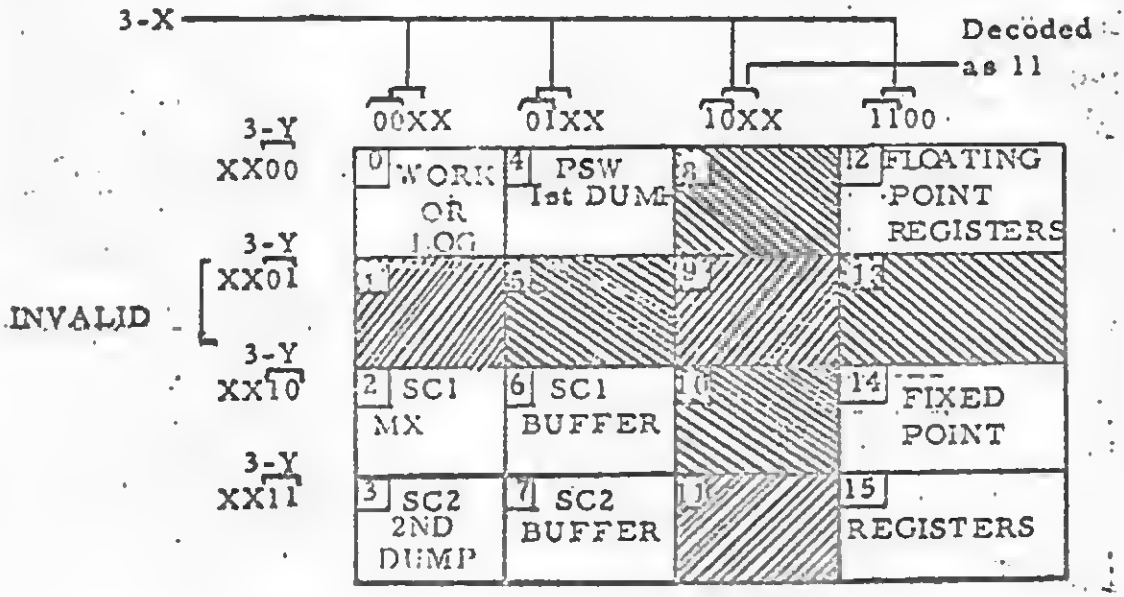
FIG.9 CARRY LOOK AHEAD DELAYS

LQ =	E0	E1	E2	Q0	Q1	Q2	Q3	E3	
LA =	0	1	0	0	E0	E1	E2	E3	
LB =	0	0	0	0	E0	E1	E2	E3	— CPU State
	0	0	1	0	E0	E1	E2	E3	— I/O State on MPX and SC1 Channels
	0	0	1	1	E0	E1	E2	E3	— I/O State on SC2 Channel

LJ =	J0	J1	J2	J3	J4	J5	E2	E3

LSAR =	0	1	2	3	4	5	6	7

S-7 ENTRY -	128	64	32	16	8	4	2	1
ADDRESS BITS								
DRIVE LINES	3-X		3-Y		4-X		4-Y	



2. Scan

On the last micro-instruction of the dump routine, an *SCA control is called in which a hardware scan of the conditions which could have caused a dump produces bit 1 and 0 of the next ROS address and sets channel selector and I/O Mode latches. The conditions and bits are as follows:

MX address in or status in	10
SC address in or status in	01
SC Data Service	11
UNDUMP	00

See Channels Section 2.

3. Dump - 2nd Level

If the SCAN results from the "MX address in or status in", a second dump can take place as a result of the "SC address in or status i or the "SC Data Service". The second dump performs the same dump as the first except the area is 0011 words 9 to 15. On cycle 1 of the 2nd dump; the DUMP 2 latch is set. At the end of this dump routine, another "scan" is performed to determine the cause of the dump.

4. Undump

Undump can occur upon completion of the service routines resulting from either a 1st level dump or 2nd level dump. It is exactly the same except for the entry micro-program which defines the area of local storage to be accessed. It also resets the appropriate Dump latch.

Cycles 1 to 6 are microprogram cycles as defined in dump-undump flow chart.

Cycle 7 - hardware controlled cycle as follows:

1. Select Local storage for read.

2. Read out location specified by J into H/J; if the Dump 1 latch is on this is location 4E; if the Dump 2 latch is on this is location 3E. This address was left in J from the previous cycle for this select.

SECTION 2.13 - LOGOUT AND ERROR HANDLING

LOGOUT

(Refer also to Vol. 4, appendix 1)

1. Logouts when enabled (ENABLE LATCH = 1) take precedence over all other possible conditions. Logouts are initiated by:

All hardware checks in CPU and Channel Microprogram of *ICC (CB=10, CD=1)
*LOG (CB=2, CD=3)

Log out results in the following sequence:

a) Recognise logout condition and stop T clock at end of T4
b) (i) Perform 12 hardware cycles in which 5 words of CPU information are stored temporarily into local storage area words 0/15 to 0/11. See page 44.
(ii) Force write back of M-7 if "READ LATCH" is on in parallel with (i).
(iii) Turn on ERR stat on first hardware cycle which prevents channel dumps as long as it is on; any error checks developed during the hardware cycles are ignored.
(iv) Read out location 0/10.
c) Perform 3 micro-program cycles in which registers A and D are stored into local storage words 0/10 and 0/9. *
d) Store into main storage by micro-program control contents of CPU and Channel data flow and local storage contents of b) (i). If the logout was initiated by a channel check, the channel causing the check is reset. See page 45. *
e) Perform CPU CHECK OUT routine. ≠
f) Perform SYSTEM RESET routine. ≠
g) Take machine check trap in which old PSW is stored at storage location 48 with a zero interruption code. The new PSW is fetched from storage location 112 during which the ERR stat is reset after the enable/disable stat has been set from bit 13 of the PSW. ≠

* A ROM parity check or ROM decoder check occurring during microprogram log-out will cause a hard stop. (stop T clock) All other errors are ignored.

≠ If a machine error is detected a hard stop will be forced.

≠ A machine error will force a hard stop until ERR is reset.

CB	CD = 3	TACT	FUNCTION
0		*STAN	Channel analyses status and forces a 4 way branch on the result.

CH	TACT	FUNCTION	LSAR CONTROL
8	EB*B	Allow other channel to break in if it is waiting for service.	
16	EB*R	If ROSCAR in control, restore control to ROAR. If ROAR in control, reset the REINTERPRET control.	

In addition, both controls load LSAR from the emit field according to the normal rules for EB type load.

CJ. One bit is added giving 8 new controls.

CJ	TACT	FUNCTION	R BUS INPUTS
EXISTING CONTROL 7 (AND Y10=0)	CIB	Channel checks and status.	
8	CST	Channel protect key to R0 0 - 3, rest 0's - CH Flag Reg. to	
9	S	Channel S register	
10	T	Channel T register	
11	W01	Buffer bytes 0, 1 to R0, 1.	
12	W2	Buffer-byte 2 to R0. Chaining boundary flags to R1 (0-4). Count Control to R1 (5-7).	
13	W34	Buffer bytes 3, 4 to R0, 1.	
14) 15)	UNUSED.		

Normally CJ = 11 gates W0 → R0, W1 → R1, unless the Read Backward latch is set in the channel, when W0 → R1, W1 → R0.

CL	TACT	FUNCTION	R BUS OUTPUTS
2	S	Channel S register	
3*	W34	Buffers 3 and 4.	